

John A. Nestor

RESEARCH INTERESTS

FPGA-Based Design and Reconfigurable Logic
Design of VLSI Circuits and Systems
Hardware Description Languages (HDLs)
Computer-Aided Design for VLSI
Applying Java and the Web to Engineering Education

EDUCATION

Ph.D. Electrical Engineering, Carnegie Mellon University, 1987
Dissertation: *Specification and Synthesis of Digital Systems with Interfaces*
Advisor: Professor Donald E. Thomas, Jr.

MSEE (Computer Engineering), Carnegie Mellon University, 1981
Thesis: *Defining and Implementing a Multi-level Design Representation with Simulation Applications*
Advisor: Professor Donald E. Thomas, Jr.

BEE (Cooperative Plan, With Honor), Georgia Institute of Technology, 1979

PROFESSIONAL EXPERIENCE

2000-present	Associate Professor Lafayette College, Easton, Pennsylvania
1995-1999	Associate Professor and Associate Chair, Computer Engineering Illinois Institute of Technology, Chicago, Illinois
1993-1995	Associate Professor and Director, Computer Engineering Program Illinois Institute of Technology, Chicago, Illinois
1987-1993	Assistant Professor Illinois Institute of Technology, Chicago, Illinois
1979-1987	Graduate Research Assistant Carnegie Mellon University, Pittsburgh, Pennsylvania
Summer 1982	Research Engineer Intel Corporation, Aloha, Oregon
Summer 1980	Research Engineer Hewlett-Packard Corporation, Cupertino, California

AWARDS AND HONORS

John A. Curtis Award, American Society for Engineering Education (ASEE) Computers in Education Division (CoED) for “the best paper presentation in the CoED sessions of the 2002 ASEE Annual Conference”, June 2003

IEEE Senior Member, 1991

Best Paper Award at the *22nd International Workshop on Microprogramming and Microarchitecture*, August 1989

Member Sigma Xi (Research Honor Society), Eta Kappa Nu (EE Honor Society), and Tau Beta Pi (Engineering Honor Society)

PUBLICATIONS

Journal Articles

J. A. Nestor, "Experience with the CADAPPLETS Project", *IEEE Transactions on Education*, Vol. 51, No. 3, pp. 342-348, August 2008.

J. A. Nestor, "L3: An FPGA-Based Multilayer Maze Routing Accelerator", *Microprocessors and Microsystems*, Vol. 29, No. 2-3, pp. 87-97, March 2005.

J. A. Nestor and G. Krishnamoorthy, "SALSA: A New Approach to Scheduling with Timing Constraints", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1107-1122, August 1993.

J. A. Nestor, "Visual Register-Transfer Description of VLSI Microarchitectures", *IEEE Transactions on VLSI Systems*, pp. 72-75, March 1993.

D. P. Lapotin, S. R. Nassif, J. V. Rajan, M. B. Bushnell, and J. A. Nestor, "DIF: A framework for VLSI multi-level representation", *Integration, the VLSI Journal*, Vol. 2, pp. 227-241, February 1984.

D. E. Thomas and J. A. Nestor, "Defining and Implementing a Multilevel Design Representation with Simulation Applications", *IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems*, Vol. CAD-2, No. 3, pp. 135-144, July 1983.

Book

D. E. Thomas, E. M. Dirkes, R. A. Walker, J. A. Nestor, J. V. Rajan, and R. L. Blackburn, *Algorithmic and Register-Transfer Level Synthesis: The System Architect's Workbench*, Kluwer Academic Publishers, 1990. Primary author of Chapter 2: "Design Representation and Synthesis", and Chapter 5, "Control Step Scheduling".

Conference Papers with Proceedings (Full Paper Peer-Reviewed)

J. A. Nestor, "Work in Progress: A New Course on Intellectual Property, Innovation, and Ethics", to appear in *Proceedings IEEE Frontiers in Education Conference*, October 2009.

J. A. Nestor and C. Nadovich, "An FPGA-Based Wireless Network Capstone Project", to appear in *Proceedings International Conference on Microelectronics Systems Education*, July 2009.

J. A. Nestor and J. Lavine, "An FPGA-Based Accelerator for Detailed Maze Routing", *Proceedings International Symposium on Field Programmable Logic and Applications*, August, 2007.

- J. A. Nestor, "Experience with the CADAPPLETS Project", *Proceedings International Conference on Microelectronics Systems Education*, June 2007.
- J. A. Nestor, "Teaching Computer Organization with HDLs – An Incremental Approach", *Proceedings International Conference on Microelectronics Systems Education*, June 2005.
- J. A. Nestor, "CADAPPLETS: Visualization of VLSI CAD Algorithms", *Proceedings 2003 International Conference on Visual Languages and Computing*, September 2003.
- J. A. Nestor, "FPGA Implementation of a Maze Routing Accelerator", *Proceedings International Conference on Field-Programmable Logic and Applications*, September 2003.
- J. A. Nestor and D. A. Rich, "Integrating Digital, Analog, and Mixed-Signal Design in an Undergraduate Curriculum", *Proceedings International Conference on Microelectronics Systems Education*, June 2003.
- D. A. Rich and J. A. Nestor, "Analog and Mixed-Signal IC Design in a Junior Electronics Course Sequence", *Proceedings ASEE Annual Conference*, June 2003.
- J. A. Nestor and D. A. Rich, "Adding Analog and Mixed-Signal Concerns to a Digital VLSI Course", *Proceedings ASEE Annual Conference*, June 2002.
- J. A. Nestor, "Animation of VLSI CAD Algorithms: A Case Study", *Proceedings ASEE Annual Conference*, June 2002.
- J. A. Nestor, "A New Look at Hardware Maze Routing", *Proceedings Great Lakes Symposium on VLSI*, pp. 142-147, April 2002.
- J. A. Nestor, "Web-Based Visualization Tools for Teaching VLSI CAD Algorithms", *Proceedings International Conference on Microelectronic Systems Education*, pp. 100-101, June 2001.
- M. Rhinehart and J. A. Nestor, "SALSA II: Improved Transformational Scheduling for High-Level Synthesis", *Proceedings IEEE International Symposium on Circuits and Systems*, pp. 1678-1681, May 1993.
- J. A. Nestor and V. Tamas, "Exploiting Scheduling Freedom in Controller Synthesis", *Proceedings Sixth International Workshop on High-Level Synthesis*, Laguna Beach, California, November 1992.
- G. Krishnamoorthy and J. A. Nestor, "Allocation using an Extended Binding Model", *Proceedings 29th Design Automation Conference*, pp. 279-284, June 1992.
- J. A. Nestor and G. Krishnamoorthy, "SALSA: A New Approach to Scheduling with Timing Constraints", *Proceedings International Conference on Computer-Aided Design*, pp. 262-265, Nov. 1990.
- J. A. Nestor, B. Soudan and Z. Mayet, "MIES: A Microarchitecture Design Tool", *Proceedings 22nd International Workshop on Microprogramming and Microarchitecture*, pp. 217-222, August 1989 (Best Paper Award).

D. E. Thomas, E. M. Dirkes, R. A. Walker, J. A. Nestor, J. V. Rajan, and R. L. Blackburn, "The System Architect's Workbench", *Proceedings 25th Design Automation Conference*, pp. 337-343, June 1988.

J. A. Nestor and D. E. Thomas, "Behavioral Synthesis with Interfaces", *Proceedings International Conference on Computer-Aided Design*, pp. 112-115, November 1986.

J. A. Nestor and D. E. Thomas, "Defining and Implementing a Multilevel Design Representation with Simulation Applications", *Proceedings 19th Design Automation Conference*, pp. 740-746, June 1982.

Conference Papers with Proceedings (Abstract Reviewed)

R. Peruzzi, M. White, D. A. Rich, J. A. Nestor, E. Geissenhainer, and M. Johnston, "An Efficient Low-Power Audio Amplifier with Power Supply Rails Tracking the Output by means of Pulse Width Modulation", *Proceedings of the Audio Engineering Society Convention*, October, 2003.

J. A. Nestor, "FPGA Implementation of a Multilayer Maze Routing Accelerator", *Proceedings 6th Annual Military and Aerospace Programmable Logic Device (MAPLD) International Conference*, September 2003.

Conference Presentations (Full Paper Reviewed)

J. A. Nestor and J. Lavine, "An FPGA-Based Accelerator for Detailed Maze Routing", *International Symposium on Field Programmable Gate Arrays*, February 2007.

Conference Presentations (Abstract Reviewed)

J. A. Nestor, K. Nasabzadeh, and O. Bowen, "Supporting Rip-Up and Reroute in an FPGA-Based Maze Routing Accelerator", *7th Annual Military and Aerospace Programmable Logic Device (MAPLD) International Conference*, September 2005.

J. A. Nestor, "Benchmark Examples with the ISYN System", *Third International Workshop on High Level Synthesis*, Orcas Island, Washington, January 1988.

J. A. Nestor and D. Thomas, "Behavioral Synthesis with Interfaces", *Second ACM/IEEE International Workshop on High Level Synthesis*, Santa Barbara, California, May 1986.

RESEARCH FUNDING

Co-PI, "Instrumentation and Laboratory Improvement: A Laboratory for Integrating Design and Test", National Science Foundation DUE-9650347, \$120,471, 1996-1998 (with M. Chang and A. Takach)

PI, "Research Initiation Award: New Techniques for High-Level Synthesis", National Science Foundation MIP-9010406, 1990-92, \$66,984

PI, "Microarchitecture Design Tools", Illinois Institute of Technology Education Research Initiative Fund, 1989-90, \$13,000

PROFESSIONAL ACTIVITIES

Senior Member, IEEE and IEEE Computer Society

Member, Association for Computing Machinery and ACM Special Interest Group on Design Automation (SIGDA)

Program Committee Member, IEEE International Conference on Microelectronics System Education, 2003, 2005, 2007, 2009

Poster Chair and Organizing Committee Member, IEEE International Conference on Microelectronics System Education, 2007

Assistant Program Chair, Poster Chair, and Organizing Committee Member, IEEE International Conference on Microelectronics System Education, 2009

Program Chair and Organizing Committee Member, IEEE International Conference on Microelectronics System Education, 2011

Technical reviewer for:

- ACM/IEEE Design Automation Conference
- The International Conference on Field Programmable Logic and Applications
- IEEE International Conference on Microelectronics System Education
- Midwest Symposium on Circuits and Systems
- *ACM Transactions on Design Automation of Electronic Systems*
- *Information Sciences* (Elsevier)
- *IEEE Transactions on CAD of Integrated Circuits and Systems*
- *IEEE Transactions on Education*
- *IEEE Transactions on VLSI Systems*
- *Microprocessors and Microsystems*
- McMillan, Inc.
- McGraw-Hill, Inc.
- Hawaii International Conference on Systems Sciences
- National Science Foundation

TEACHING CONTRIBUTIONS**Courses Taught at Lafayette College 2004-2009**

Fall 2009

ECE 211 Introduction to Digital Circuits (Lecture + 2 sections Laboratory)

ECE 491 Senior Design project 1 (Lecture + Laboratory)

Spring 2009

ES 225 Engineering Professionalism and Ethics
ECE 313 Computer Organization
Fall 2008
ECE 491 Senior Design project 1 (2 Sections Lecture + Laboratory)
Spring 2007
ECE 425 VLSI Circuit Design (Lecture + Laboratory)
Fall 2007
ECE 211 Introduction to Digital Circuits (Lecture + 2 sections Laboratory)
ECE 491 Senior Design project 1 (Lecture + Laboratory)
Spring 2007
VAST 200 Computers and Society
ECE 425 VLSI Circuit Design (Lecture + Laboratory)
Fall 2006
ECE 313 Computer Organization
ECE 491 Senior Design Project 1 (Lecture + Laboratory)
Spring 2006
Sabbatical Leave
Fall 2005
ECE 211 Introduction to Digital Circuits (Lecture + Laboratory)
ECE 491 Senior Design Project 1
Spring 2005
VAST 200 Computers and Society
ECE 425 VLSI Circuit Design (Lecture + Laboratory)
Fall 2004
ECE 313 Computer Organization
ECE 491 Senior Design Project 1 (Lecture + Laboratory)
Spring 2004
VAST 200 Computers and Society
ECE 425 VLSI Circuit Design (Lecture + Laboratory)
Course Taught at Lafayette College (2000-2003)
ECE 211 Introduction to Digital Circuits (Lecture + Laboratory)
ECE 313 Computer Organization
ECE 323 Analysis and Design of Solid State Circuits (Laboratory)
ECE 425 VLSI Circuit Design (Lecture + Laboratory)
ECE 426 VLSI System Design (Lecture + Laboratory)

Courses Taught at Illinois Institute of Technology (1987-2000)

ECE 111/112	Introduction to Computers & Engineering I, II
CPE 101	Introduction to the Profession II
ECE 228	Digital Design
ECE 242	Computer Organization and Programming
ECE 429	Introduction to VLSI Design
ECE 446	Logic Design & Implementation
ECE 448	Mini/Micro Computer Programming (UNIX/C Programming)
ECE 449	Object-Oriented Programming and Computer Simulation (Java)
I PRO	Interprofessional Project - Web-Based Image Capture to Augment the IITV Distance-Learning Network
I PRO	Interprofessional Project - A Website for the Kevin Uliassi's Around-the-World Balloon Flight
ECE 497	VLSI Prototype Testing
ECE 530	VLSI Design
ECE 588	CAD Algorithms for VLSI
ECE 748	Introduction to Java Programming for Engineers (Short Course)

Students Supervised**Ph.D. Thesis (at Illinois Institute of Technology)**

- K. Rajan, "A New Approach for Testing Sequential Circuits", May 1996. This work was jointly supervised with Dr. Miron Abramovici, Adjunct Associate Professor of ECE and Distinguished Member of Technical Staff at Bell Laboratories, Murray Hill, New Jersey.
- P. Parikh, "Sequential Test Generation for VLSI Integrated Circuits", May 1996. This work was jointly supervised with Dr. Miron Abramovici, Adjunct Associate Professor of ECE and Distinguished Member of Technical Staff at Bell Laboratories, Murray Hill, New Jersey.
- M. Iyer, "Redundancy Identification and Removal in Sequential Circuits", May 1995. This work was jointly supervised with Dr. Miron Abramovici, Adjunct Associate Professor of ECE and Distinguished Member of Technical Staff at Lucent Technologies, Murray Hill, New Jersey.
- V. Tamas, "Controller Synthesis from Microarchitecture Specifications", December 1994.
- B. Soudan, "MIES - A Visual Register-Transfer Description (VRTD) Language for the Microarchitecture of VLSI Systems", August 1994.
- P. Yuan, "Multiple Connected Parallel Pipelined Machine: A New Microarchitecture with Multiple Connected Parallel Pipelined Execution Units", December 1993.
- G. Krishnamoorthy, "SALSA: A New Approach to High-Level Synthesis", September 1992.

MS Thesis Completed (at Illinois Institute of Technology)

- M. Rhinehart, "SALSA-II: A Transformational Scheduling Algorithm for High-Level Synthesis", December 1994.
- N. Hassan, "Speed Up Techniques for Test Generation Algorithms", December 1992. This work was jointly supervised with Dr. Miron Abramovici, Adjunct Associate Professor of ECE and Distinguished Member of Technical Staff at AT&T Bell Laboratories, Naperville Illinois.
- A. Farrahi, "An Interface Between the RTL Description and Physical Layout Description of a Digital System", December 1992.
- J. Hoff, "The VLSI Implementation of the Superimposed Random Coding Artificial Neural Model", May 1992. This work was jointly supervised with Professor P. Greene of the Computer Science Department.
- M. Iyer, "One-Pass Redundancy Identification and Removal in Combinational Circuits", December 1991. This work was jointly supervised with Dr. Miron Abramovici, Adjunct Associate Professor of ECE and Distinguished Member of Technical Staff at AT&T Bell Laboratories, Naperville Illinois.
- A. Bakthavathsalu, "Scheduling under Timing Constraints using Constraint Satisfaction", September 1991.
- I. Goodman, "LSTI: A Logic Synthesis Tool Interface for the System Architect's Workbench", 1989.

BS Honors Thesis Projects (at Lafayette College)

- R. Umbrasas, "Cellular Automata on an FPGA: Performance and Cost Analysis", 2010.
- W. B. Towne, "Cellular Automata on an FPGA: A Special-Purpose Processor for Discrete Deterministic Systems", 2009.
- S. Nowlan, "An FPGA-based Implementation of the AES Encryption Standard" (co-advised with Professor John Greco), 2007.
- J. Lavine, "A Routing Accelerator for FPGAs", 2007.
- O. Bowen, "High Level Control of an FPGA Maze Routing Accelerator", 2005.
- K. Nasabzadeh, "Extensions to Direct Grid Maze Routing Accelerators", 2005.
- E. Geissenhainer, "A General Purpose Very Efficient Amplifier" (co-advised with Professor David A. Rich), 2004.
- W. Sutey, "FPGA Implementation of a 32-bit RISC Pipelined Microprocessor" (co-advised with Professor William A. Hornfeck), 2004.
- M. Johnston, "A Digital Control Chip for a PWM Amplifier" (co-advised with Professor David A. Rich), 2003.

Undergraduate Projects (at Lafayette College)

- B. Ilbeyi, "Visualization Applets for Computer Architecture", EXCEL Research Project, Summer 2009.

- C. Dionisio, "FPGA-Acelerated Pattern Routing", EXCEL Research Project, Summer 2008.
- J. Letoski, "An FPGA Routing Accelerator", EXCEL Research Project, Summer 2007.
- J. Lavine, "Improvements to the L4 Hardware Routing Accelerator", EXCEL Research Project, Interim Session 2006 and Spring Semester 2006.
- J. Mumo, "Visualization Tools for VLSI CAD Algorithms", EXCEL Research Project, Summer 2005.
- K. Nasabzadeh, "Implementation and Evaluation of a Maze Routing Accelerator", EXCEL Research Project, Summer 2004.
- O. Bowen, "Visualization of Register-Transfer Level Designs", EXCEL Research Project, Summer 2003.
- M. Johnston, "Implementation and Evaluation of a Hardware Accelerator for Maze Routing", EXCEL Research Project. Summer 2002.
- A. Carle, "VHDL Design of a MIPS Processor Subset for FPGA Implementation", Senior Project, 2001-2002.
- R. Czarnecki, "Visualizing Register Transfer Designs", EXCEL Research Project, Interim Session 2002.
- M. Marbell, "Software Implementation of the Lee Routing Algorithm", EXCEL Research Project, Fall 2001.
- F. Laiwalla, "Visualization Tools for Teaching VLSI CAD Algorithms", EXCEL Research Project, Summer 2001.
- V. Oktem, "Web-Based Remote Testing of Student VLSI Chip Designs", EXCEL Research Project, Summer 2001.
- R. Niewoehner, "VHDL-Based Design of a Single-Cycle MIPS Processor for FPGA Implementation", Senior Project, 2000-2001.

Undergraduate Projects (at Illinois Institute of Technology)

- G. Morales, "Converting the J. Renee Website for Standalone Operation", Spring 1999.
- F. Martinez, "Web-based advising tools", Spring 1999.
- T. Ihimoyan, "Software and Hardware Implementation of Maze Routing", Summer-Fall, 1998.
- L. Covaci, "Digital Design Experiments using ABEL PLD Software", 1 cr., Fall 1996.
- A. Solarik, "Image Capture Techniques to Augment the IITV Distance-Learning Network", Spring 1996.
- P. Bhargava, "A Prototype Web Page Interface to Augment the IITV Distance-Learning Network", 2 cr., Spring 1996.
- S. Ghassemi, "A Graph-Drawing Program to Support High-Level Synthesis", 3 cr., Fall 1995.

- D. Mustea, "Interfacing a CCD Camera to a PC", 3 cr., Spring 1994.
A. Bakh, "Digital Design Experiments", 1 cr., Fall 1993.
I. Bhatti, "Towards Developing a Multimedia Instructional Laboratory", 3 cr., Fall 1993.
T. Coduto, "Developing a Laboratory for VLSI Design", 3 cr., Fall 1991.
A. Pulikowski, "Display Board for Non-Verbal Communication", 1 cr., Spring 1991.
Y. Kim, "A Visual Model of the DLX Computer Architecture", 2 hr, Fall 1990.
G. Shapkarov, "ASIC Design using LEdit Place & Route Software", 3 cr., Fall 1990.
T. Mallick, "A Graph Drawing Package for the Sun Workstation", 3 cr., Spring 1990.
T. Gustafson, "Design using CapFast CAD Package", 1 cr., Spring 1990.
V. Truong, "A SCSI Interface for the Commodore Amiga", 3 cr., Spring 1989.
K. Lay, "Logic Design with Xilinx Field-Programmable Gate Arrays", 3 cr., Spring 1989.
J. Chow, "Traffic Light Controller PLD Implementation", 1 cr., Spring 1989.
D. Nguyen, "Pretesting EE 446 Lab Experiments", 1 cr., Summer 1988.
H. Sahouri, "A Measurements Package for the Systems Architect's Workbench", 3 cr., Spring 1988.

SERVICE

Service at Lafayette College

Information Technology Advisory Committee, 2004-2009 (Secretary, 2006-2007, Chair 2007-2009)

Search Committee for Director of Engineering, Spring 2008.x

Faculty Compensation Committee, 2002-03

Women's Studies Advisory Committee, 2002-2005

Faculty Advisor for Lafayette Chapter of Eta Kappa Nu (ECE Honor Society), 2002-2005

Computer Science Department Search Committee for Visiting Instructor, Fall 2002

Engineering Division Committee to Review *ES 225 – Ethics and Professionalism*, Fall, 2001

Skillman Library Search Committee - Access Services Librarian, Fall 2001

Service at Illinois Institute of Technology

Faculty Representative at IIT Trustee Retreat, 1999

University ABET 2000 Steering Committee, 1999

Department Academic Discipline Committee, 1998-99

ECE Department Chair Search Committee, 1997-99
CS Department Chair Search Committee, 1998-1999
Filmer Endowed Chair Search Committee, 1998-99
Academic Computing Subcommittee of Faculty Council, 1990-92, 1996-98
(Chair 1997-98)
Undergraduate Admissions Oversight Committee, 1997-99
University DoD Computing Grant Steering Committee, 1996-97
Faculty Representative, Trustee Task Force on Information Technology, 1996
University ABET Steering Committee, 1995-96
University Undergraduate Studies Committee, 1995-99
University Search Committee for Director of Computing, 1995-96
University DoD Computing Grant Workstation & Visualization Committee, 1994-99
Chair of Department Committee to propose a BS in Computer Engineering, 1992-93
Department Curriculum Committee, 1987-1996
Department Faculty Coordinator of Computer Engineering Courses, 1989-99
ECE/CS Committee to Develop MS in Computer Systems Engineering, 1990
Armour College Committee on Freshman Recruiting and Curriculum, 1988
University Committee to Review Copyright Policy, 1988
Faculty Adviser for IIT Chapter of Eta Kappa Nu (EE Honor Society), 1988-90