1. Parasitic Calculations 10 Points

(a) Calculate the parasitic resistance and capacitance of the poly wire shown above.

\[ R = \] 

\[ C = \] 

(b) Calculate the parasitic capacitance due to the transistor gates of the inverter.

\[ C = \]
2. Logic Gate Circuit Design 10 Points

In the space provided below, draw a transistor-level circuit diagram that includes the NOR gate, the parasitic resistance and capacitance of the polysilicon wire, and the inverter. Label your diagram with to show parasitic values for both the polysilicon wire and the inverter gate capacitance.

3. Delay Calculations 20 Points

Calculate the rise time and fall time of the NOR gate taking into account the parasitic capacitance of the inverter AND the parasitic capacitance and resistance of the polysilicon wire. Hint: lump together the inverter gate capacitance and the polysilicon wire capacitance.

\[ t_r = \]

\[ t_f = \]
4. Testing 20 Points

A simple combinational gate circuit is shown below. We want to generate tests for a stuck-at-0 fault on node N1 and a stuck-at-1 fault on node N2.

(a) Write the input conditions necessary to sensitize a stuck-at-0 fault on node N1.

(b) Write the input conditions necessary to propagate a stuck-at-0 fault on node N1 to the output.

(c) Write the input conditions necessary to sensitize a stuck-at-1 fault on node N2.

(d) Write the input conditions necessary to propagate a stuck-at-0 fault on node N2 to the output.

5. Routing 20 Points

A routing channel is shown below with net terminals marked at the top and bottom of the channel.
(a) List the nets in order of left edge.

(b) Mark the assignment of nets to tracks and the connections between nets and terminals that will result from the Left Edge Algorithm (draw the connections directly on the diagram).

(c) What is the density of this routing channel?

(d) Does this routing channel contain any vertical constraints? Why or why not?

6. Combinational Logic Design Using VHDL 20 Points

The VHDL code below implements a simple logic function:

```vhdl
Library IEEE;
use IEEE.std_logic_1164.all;

entity test_ckt is
  port(
    x : in std_logic_vector(1 downto 0);
    enb : in std_logic;
    a : in std_logic;
    b : in std_logic;
    c : in std_logic;
    d : in std_logic;
    y : out std_logic;
  );
end;

architecture logic of test_ckt is
begin
combin: process(x, enb, a, b, c, d)
begin
  y <= '0';
  if (enb = '1') then
    case x is
    when "00" => y <= a;
    when "01" => y <= b;
    when "10" => y <= c;
    when "11" => y <= d;
    when others => y <= '0';
    end case;
  end if;
end process;
end logic;
```
(a) Draw a block diagram showing the inputs and outputs of the VHDL module as a “black box”.

(b) Write the equation of this circuit as a Boolean logic function.

(c) What is the name of this circuit function?