1. Complementary CMOS Logic 20 Points

The diagram below shows the pull-down network of a complementary CMOS logic circuit.

(a) Draw the proper pull-up network for this circuit in the box provided.

(b) Write the logic equation of this circuit:

2. Complementary CMOS Design 20 Points

(a) Draw the schematic diagram of a 3-input CMOS NOR gate and sketch a layout using a stick diagram in the space provided below.
(b) Assume that for the both P-transistors and N-transistors in the NOR gate \( W=8.0\mu m \) and \( L=2.0\mu m \) and that the load capacitance on the output is “arbitrary large”. Use the design equations in Chapter 2 to calculate the maximum current that can flow to the GND power supply connection during a H-L transition on the output.

3. Current Density 10 Points

Assume that the ground connection for the NOR gate in problem 2 is made using a minimum-size metal wire using SCMOS design rules.

(a) What is the maximum current that can be safely pass through this wire?

(b) Is the minimum-size wire sufficient for the NOR gate in problem 2? Why or why not?

4. Delay Calculation 20 Points

Assume that the dimensions of the transistors in the diagram shown above are:

\[ W_{n1}=3\lambda, \ L_{n1}=2\lambda, \ W_{p1}=8\lambda, \ L_{p1}=2\lambda, \ W_{n2}=9\lambda, \ L_{n2}=2\lambda, \ W_{p2}=24\lambda, \ L_{p2}=2\lambda \]
(a) Calculate the value of the capacitance seen at the output of the first inverter due to the gate capacitance of transistors in the second inverter (i.e., p2, n2).

(b) Calculate the rise time and fall time of inverter 1 using the capacitance value you calculated in (a).

(c) Calculate the rise time and fall time of the inverter 2 given the external load.

(d) Calculate the worst-case total delay of the two inverters from a change on the input IN to a change on the output OUT.

5. Parasitic Calculation 20 Points
Consider the Magic layout fragment shown above, which shows a grid of one lambda. Calculate the parasitic resistance and capacitance values for the different parts of the layout and draw a schematic diagram showing the parasitic values. Hint: break the layout up into rectangular areas, then calculate the parasitic values for each area.

6. Latch Operation

Fill in the timing diagram below to demonstrate the operation of the two latches in the schematic diagram above.

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