Problems 1-3 refer to the transistor-level schematic diagram shown below:

1. **CMOS Combinational Networks**  
   10 Points

Draw a gate-level schematic that corresponds to the schematic above, showing primitive static CMOS gates and their interconnections.
2. Delay Calculation 20 Points

Given the load capacitance $C_L$ on the output and assuming that all transistors are sized with $W=5\lambda$ and $L=2\lambda$, calculate the worst-case delay between a change on the inputs $A$, $B$, $C$, or $D$, and a change on the output. Assume that all loading in the first gate is due to transistor-gate parasitic capacitance – neglect all interconnect parasitics.

3. Testing 20 Points

(a) Show the input conditions necessary to test for a stuck-at-0 fault on node $X$ in the diagram shown above. Note what the correct output and faulty outputs will be when this test is applied.

(b) Show the input conditions necessary to test for a stuck-at-1 fault on node $X$ in the diagram shown above. Note what the correct output and faulty outputs will be when this test is applied.
4. Dynamic Logic 20 Points

(a) Re-implement the gate shown in Problem 1 using domino logic.

(b) Compare the number of transistors (n-type AND p-type) required for this gate to the number of transistors required for the static CMOS implementation shown in problem 1).

(c) Suppose that the inputs of your logic gate are set so that A=0, B=0, and C=1, and also so that D alternates between 0 and 1 at an average frequency of 100KHz. Assume further that the precharge clock Ø operates at a frequency of 1MHz. What will the power consumption of the dynamic gate be under these conditions as a function of load capacitance \( C_L \) and power supply voltage \( V_{dd} \)? Compare this value to the power consumption of the static CMOS implementation.
5. Channel Routing – Left Edge Algorithm 15 Points

A routing channel is shown below with net terminals marked at the top and bottom of the channel.

(a) List the nets in order of left edge.

(b) Mark the assignment of nets to tracks and the connections between nets and terminals that will result from the Left Edge Algorithm (draw the connections directly on the diagram).

(c) What is the density of this routing channel?

(d) Does this routing channel contain any vertical constraints? Why or why not?
6. VHDL Coding

The VHDL code below implements a simple logic function:

```vhdl
Library IEEE;
use IEEE.std_logic_1164.all;

entity testckt is
  port(
    i1, i2 : in std_logic_vector(3 downto 0);
    output : out std_logic_vector(3 downto 0)
  );
end;

architecture behavior of testckt is
begin
  combin: process ( i1, i2 )
  begin
    if (i1 < i2) then output <= i1;
    else output <= i2;
  end if;
end process combin;
end;
```

(a) Draw a block diagram showing the inputs and outputs of the VHDL module as a “black box”. Use the back of this page if you want to.

(b) What will the function of this circuit be if i1="0111" and i2="1110"?

(c) Briefly describe in words the function of this circuit.