1. **CMOS Gate Design / Layout**  
   **20 Points**

In this problem, we will consider the design of a 3-input NAND gate.

(a) Draw a transistor-level schematic diagram of a 3-input NAND gate in the space provided below:

![Schematic Diagram](image)

(b) Sketch a sticks diagram of a layout for the 3-input NAND gate that meets the following requirements and minimizes overall cell height:

1. Vdd and Gnd run through the top and bottom of the cell, respectively on metal 1.
2. Input terminals A, B, and C are in metal 1 on the left edge of the cell (order is not important),
3. Output OUT is in metal 1 on the right edge of the cell
2. Delay Calculation  

In this problem, we will assume that the NAND gate discussed in Problem 1 is designed with minimum-sized transistors and has an output load of 30fF, as shown below.

(a) Calculate the worst-case \textit{rise time} of this gate, \( t_r \)

(b) Calculate the worst-case \textit{fall time} of this gate, \( t_f \)

(c) Suppose that we want the worst-case rise time and fall time of this gate to be approximately equal. Which transistors in the gate should be resized, and what should their new dimensions be? Be careful … transistors must follow design rules!
3. Magic Layout / Parasitic Calculations 30 Points

This problem concerns the Magic layout fragment shown below, which contains a transistor and some additional layout objects:

(a) Calculate the parasitic resistance of the layout object between labels A and B.

(b) Calculate the parasitic capacitance of the layout object between labels E and F.

(c) Calculate the parasitic capacitance of the layout object shown between labels B and C and F and G

(d) Draw a schematic diagram showing how the parasitic values that you calculated in parts (a)-(c) above relate to the transistor (i.e., which transistor terminal each parasitic component connects to).
4. Power Consumption 20 Points

A significant amount of power is consumed in the distribution of clock signals that drive a VLSI circuit. To reduce power consumption, some circuits are designed with a “Standby” mode in which the clock signals for unneeded functions are temporarily disabled. When the functions are needed again, the clock signals are enabled again.

The figure below shows the basic idea: critical functions which are never suspended are attached to the clock signal “CLK1”, which is never disabled. Functions which are to be suspended during “Standby” mode are attached to clock signal “CLK2”, which is disabled when the CLKEN enable signal is a logic low.

Assume for this problem that the power supply voltage \( V_{DD} = 3.3 \text{V} \) and clock frequency \( f_{clk} = 100 \text{MHz} \).

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\begin{align*}
C1 &= 300 \text{fF} \\
C2 &= 600 \text{fF}
\end{align*}
\]

(a) What is the power consumption of this circuit when CLKEN=1?

(b) What is the power consumption of this circuit when CLKEN=0?

(c) What percentage of power is saved when the circuit is in “Standby” mode (i.e., CLKEN=0)?