1. **Sequential Circuit Design**  
   25 Points

(a) Draw a transistor-level schematic diagram of this circuit in the space provided below.
(b) What is the logic function performed by this circuit?

(c) Is this circuit dynamic, static, or pseudo-static?

(d) What is the function of the input E?

2. **Sequential Circuit Timing**  
   15 Points

Fill in the timing diagram below to show the operation of the circuit shown on page 1.

```
phi1bar
phi1
phi2
phi2bar
D
E
S1
Qb
S2
Q
```
3. Testing  

Consider the logic circuit shown below:

(a) What input values are necessary to test for a stuck-at-0 (S-A-0) fault on node P?

(b) What input values are necessary to test for a stuck-at-1 (S-A-1) fault on node G?

4. Combinational Design with Verilog (3.2)  

This problem refers to the Verilog module shown below:

```verilog
module comb_logic(a, b, out, oflo);
    input [7:0] a, b;
    output [7:0] out;
    reg [7:0] out;
    output oflo;
    reg oflo;
    reg [7:0] s;

    always @(a or b)
    begin
        {oflo,s} = a + b;  // oflo gets "carry out"
        if (oflo) out = 8'hFF;
        else out = s;
    end
endmodule
```
(a) Draw a “high-level” block diagram of the hardware which will be synthesized by this Verilog description (i.e. input & output ports, adders, multiplexers, etc.)

(b) What function is performed by this circuit?

5. **Sequential Design with Verilog (3.2)**

Write a Verilog description of a FSM that implements the state diagram shown below with a single input \( X \) and a single output \( Y \). Note: transitions marked with “-“ are always taken.